ABSTRACT

A frequency divider has two or more storage elements connected in a loop. One of the outputs of each storage element is connected to one of the inputs of another storage element. Each storage element provides at least one output signal having a period equal to the period of a reference input signal multiplied by the number of interconnected storage elements. The reference input signal may be, for example, a local oscillator ("LO") signal. In the case where the reference input signal has a 50% duty cycle, the output signals will also have a 50% duty cycle. Furthermore, in the case where a total of three storage elements are connected in a loop, the outputs of two of the three storage elements can be combined to provide a signal having substantially no third order harmonics.